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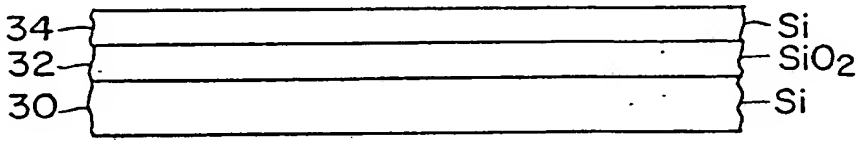

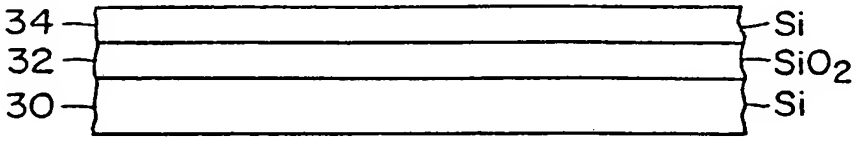

(57) Abstract

An improved method of zone-melting and recrystallizing of polysilicon film on an insulator over silicon is described.

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ZONE-MELTING RECRYSTALLIZATION PROCESS

Description

Background Art

Zone-Melting Recrystallization (ZMR) is a process for producing thin crystalline films of silicon (Si) isolated from a silicon substrate by a buried insulating layer, i.e., SiO_2. In the ZMR process a layer of SiO_2 is deposited on a substrate, often a single-crystal wafer. Polycrystalline Si (polysilicon) is then deposited on the SiO_2 layer; followed by deposition of a capping layer or a wetting agent, such as SiO_2.

This structure is then subjected to a heat treatment wherein the polysilicon film is melted. Typically, the heating is performed using a stationary bottom heater adjacent the substrate surface. The stationary heater elevates the temperature of the polysilicon to about 1000°C-1300°C, near its melting point. A movable upper heating source is then translated past the structure adjacent the capping film to supply sufficient heat to melt the polysilicon as the heating source moves along its path. Upon recrystallization the polysilicon film is transformed to a single, or nearly single crystalline film. Optionally, a single crystal seed material may be used to aid in epitaxial recrystallization. (See U.S. Patent No. 4,371,421 to Fan et al., and "Silicon Graphoepitaxy Using a Strip-Heater Oven" by M. W.

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Geis et al., Appl. Phys. Lett., 37 (5) Sept. 1, 1980).

Silicon-on-Insulator material (SOI) prepared by the ZMR technique promises to satisfy the material needs for many important device applications, including radiation-hardened circuits, high voltage circuits, faster computating circuits, and microsensors, etc. Currently, however, ZMR processed SOI wafers have several significant material problems that can potentially limit their wide-spread adoption. The major problems are associated with one or more of the following: surface-edge defects, sub-boundary defects, surface defects, and "warp and slip".

Disclosure of the Invention

An improved process of ZMR is provided wherein the conventional single upper movable heater is supplemented by lateral fore and aft heaters to provide a shallow thermal gradient. Additionally, defect entrainment strips are formed on the upper encapsulating film so that after ZMR the entrapped defects can be located by etching away the strips. Once located, the defect area is amorphized and re-grown as single crystal defect-free material from the sides. These and other improvements will be described in connection with the drawings. In an optional embodiment, the entrainment strips are not employed and defects are not entrained. Instead, defects are optically located and, once located, the

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regions are amorphized, as above, and regrown from the sides to be defect-free.

Detailed Description of the Drawings

Fig. 1 is a partially cut-away illustration of the ZMR heaters.

Figs. 2-5 are successive schematic cross-sectional views of the ZMR process.

Fig. 6 is a flow chart of the improved ZMR process.

Fig. 7 is a transmission-electron micrograph of a cross-sectional area of Si or SiO_2 showing elimination of defects.

Detailed Description of the Invention

Surface-edge defects are caused by overheating around the edge of a wafer. Under uniform bottom-heater conditions, the upper heater often heats the edges much hotter. The overheating causes the wafer edges to melt and thus produce detrimental effects to photolithography. This is a problem even without seeding. If seeding is used, and the seeding is often done along the edges, the seeding areas (either by scribing, or photolithography) will also often cause either overheating, or other cosmic surface effects, thus affecting device photolithography.

The exact nature of the sub-boundary defects is not known. They may be attributable to thermal or mechanical vibrations in the ZMR process coupled with the sharp thermal gradients, and oxygen presence in

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the wafers. Nevertheless, it has been observed that the sub-boundaries currently disappear with Si layers thicker than 5 microns, and these sub-boundaries are replaced by dislocation arrays, still located approximately where the sub-boundaries were. The dislocation densities (estimated to be 10^5-$10^6 cm^{-2}$) are mostly threading dislocations. In between these regions, the Si film was found to be essentially defect-free. Sub-boundaries have detrimental effects on gate oxidation and leakage currents in devices. Threading dislocations usually have less detrimental effects than sub-boundaries for devices. However, they still may have detrimental effects on yields in circuits.

Protrusions are surface defects usually located at the sub-boundaries or grain boundaries. Surface protrusions (usually about a few microns across) have adverse effects on photolithography and gate oxidation during device processing.

ZMR wafers often exhibit "slips" in the wafers. They appear to be caused by sharp thermal gradients present in the typical ZMR process. These "slips" are measured to be about a few hundred Å in ZMR samples, causing possible photolithography problems. The "warps" also appear to be caused by the sharp thermal gradients. They are measured to be tens of microns across a 4" or 5" - diameter wafer.

The present invention comprises a series of processing steps which can be combined to provide much improved ZMR wafers and higher processing yield.

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Inclusion of some or all the steps is a matter of choice depending upon the particular requirements. The improvement steps are as follows:

I. Edge Effects

A quick and easy method for reducing edge effects is to cut the ZMR wafers to a smaller size, thus eliminating all the edge effects. For example, a 5"- diameter wafer can be obtained by trimming a 6"- diameter wafer. The cutting method can be either laser, mechanical, dry or wet chemical etching or ultrasonically. Sand blasting is also very effective. The detailed sand blasting process is outlined as follows:

A ZMR processed wafer is mounted on a jig and Al_2O_3 powder blasted at a velocity of about 0.02m/sec, with Al_2O_3 powder of 27 micron sieve size. The Al_2O_3 is ejected from a nozzle of about 35 mil diameter with a pressure of 80 PSI. The important wafer surface i.e. the wafer area away from the edge, is protected by a coating of photoresist, or some other resilient material. The wafer is placed about 250 mil from the nozzle. The actual cutting time is less than 90 seconds. By cutting off the edges, desirable stress relief effects have also been observed, and warping is significantly reduced.

II. ZMR Layer Thinning

Currently sub-boundaries occur in Si films of less than 0.5 microns in thickness. It is therefore desirable to prepare ZMR samples with Si films

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greater than 0.5 microns thick so as to obtain films without sub-boundaries. The thick film is then thinned down for actual device applications. In some device applications, especially for large-scale integrated circuits with small device geometries, a thin Si film is preferred having a thickness of less than 0.3 microns. Thinning the films is preferably accomplished by polishing as follows: The polishing powder used is Syton, with adhesive backing to a polishing pad. A very smooth parallel plate polishing technique must be used to assure a parallel Si film after polishing. Usually polishing also removes and reduces surface protrusion effects. Alternatively, reducing Si film thickness is accomplished by oxidation followed by etching. Either high pressure or low pressure oxidation is employed. The oxidation process must be carefully carried out to retain surface smoothness and uniformity. It can be done with steam oxidation at 950°C, or a dry oxidation in oxygen at 1200°C. With dry oxidation, the oxidation rate is about 4000A of SiO_2 in 3.5 hours. There is another advantage to dry oxidation; in that it may be combined with high-temperature annealing (to be described later).

For other device applications, such as bipolar, thick films are acceptable, and no thinning is needed.

III. Warp & Slip

To reduce warping and slips, a shallow thermal gradient method is used. Shallow thermal gradients

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are obtained by using two additional upper heaters 14 and 16 (See Fig. 1) laterally disposed before and after the movable upper heater 12 and translatable therewith.

These two additional upper heaters ideally should be separately thermally controlled and of substantially greater lateral width than the thin single upper heater to provide more symmetrical thermal input in the ZMR process, allowing better process control.

IV. Si Material Defect Reduction

In ZMR films, as above noted, sub-boundaries and threading dislocations are often observed. The exact causes of such crystal defects have not been established. However, it is known that they are present in locations where the recrystallized films are the last to solidify. Previously, the sub-boundaries or dislocations have been entrapped into preselected locations. (See, for example, U.S. Patent No. 4,479,846 to Smith et al. issued 30 Oct. 1984, which teaches use of an artificial pattern to entrain boundaries.) One such pattern may comprise a periodic raised structure of parallel strips in the underlying SiO_2 of the SOI structure. This makes the Si films along these raised structures slightly hotter than the adjacent areas, and thus they become the last area to solidify. Therefore, by having a periodic SiO_2 structure, the dislocations or sub-boundaries are localized in preselected areas.

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Unfortunately, the raised structure in the underlying SiO_2 also causes the Si films to have undulating features, which are very detrimental to device fabrication.

Another technique of entrainment is shown in Smith et al. above. In Smith et al. parallel strips of material are formed on the encapsulating layer over the polysilicon. The strips may either be a reflectional coating to thermal or light radiation or may be an absorber. In this former case, the sub-boundaries or defects are entrained away from the shaded strips and in the latter are entrained beneath the strips.

V. ZMR Process

Referring now to Fig. 1 the process and apparatus for improved ZMR will be described in more detail in connection therewith.

In the partially exploded view of Fig. 1, and the successive sectional views of Figs 2-5, and process chart of Fig. 6, the basic concepts of improved ZMR are shown. A sample wafer 10 is subjected to a thermal treatment by being disposed on a stationary lower strip-heater 11 while a movable upper strip heater 12 is mechanically translated past the sample 10 in the direction of the arrows. In accordance with the present invention fore and aft heaters 16 and 14 respectively are mechanically coupled to the conventional upper heater 12 and are mechanically translatable therewith. For example,

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rods or pins 22 may be used to couple the heaters together. Leads 26 and 28 are coupled to heat control unit 20 so that the temperature of heaters 14 and 16 may be controlled separately from each other and from the other units. The purpose of heaters 14 and 16 is to provide a less abrupt, more shallow, thermal gradient as the main upper strip heater 12 is translated past the sample. For example, if the lower heater is maintained at 1100°C the upper heater 12 is set at about 1600°C while the fore heater 16 is at 1300°C and the aft heater at 1400°C.

Under these conditions the top wafer surface first sees a temperature of about 1300°C before encountering the elevated temperature of the main heater 12.

The wafer 10 is preferably comprised of a single crystal Si substrate 30 upon which a thermally grown layer 32 of SiO_2 is formed. (Step 1 Fig. 6) A thin film of polysilicon 34, to be recrystallized, is then deposited on the SiO_2 film 32. (Step 2 Fig. 6 and Fig. 2). An encapsulation or wetting agent layer 36 of SiO_2 (or Si_3N_4, or both) is formed, as by deposition. (Step 3 Fig 6) An entrainment pattern of raised strips 38, which may preferably be periodic in nature, is then formed on, or in, the encapsulation layer 36. Preferably these strips are formed by etching away SiO_2 material from layer 36 between the desired strip locations. (Step 4 Fig 6). The structure at this point is shown in the section of Fig 3 and has the advantage that, when the wafer SiO_2 layer 36 is subsequently removed by etching; a planar upper

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layer of Si is left. (See Fig. 5).

The structure thus formed is then subjected to the ZMR process; (Step 5 Fig 6) whereby a molten zone 18 is created in the polysilicon film 34. This molten zone is moved in a direction parallel to the axis of the entrainment pattern as shown by the arrows in Fig. 1. The molten zone is long and narrow with its long axis perpendicular to the lines of the entrainment pattern. As the molten zone recrystallizes, the polysilicon film 34 is transformed to single crystal, or nearly single crystal silicon, with crystal defects 40 primarily located beneath the strips 38 (See Fig 3).

The structure shown in Fig. 3 is then subjected to a high temperature anneal in an oxygen ambient at about 1200-1300°C. Low angle grain boundaries, or sub-boundary, defects are reduced by this treatment; that is, individual sub-grains are better aligned with each other. In addition, stacking faults and twins are found to be eliminated or much reduced with this annealing step. Using X-ray rocking curve measurement, the FWHM (full-width-half-maximum) was measured to decrease from 140 arc-second to 20 arc-second after annealing in oxygen ambient at 1200°C for 1 hour. The narrow FWHM indicates a much improved crystallinity in the samples. However, threading dislocations and sub-boundaries that originate and end on both overlying and underlying

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SiO_2 interfaces cannot be annealed off. They are eliminated by the following procedure: (Step 6 Fig 6)

The strips 38 in the encapsulating SiO_2 layer 36 are etched away to expose the upper surface 42 of the recrystallized Si film 34 at the localized area of the defects. (See Fig. 4 and Step 7 Fig 6)

The next step is to amorphize the Si region underlying the exposed upper surface by providing an ion implant of Si sufficient to amorphize the exposed Si strips 42. For this purpose, $^{30}Si^+$ ions are preferably used as implantation species so as to avoid N_2^+ and CO^+ impurity ion implantations. Typically, for a 0.5 micron Si layer, a complete amorphization occurs at a dose equal to or higher than $1 \times 10^{16} cm^{-2}$ for 200 keV ions. (Step 8 Fig 6) Note that the regions on each side of the amorphized area are protected from amorphization by the remaining portion of the SiO_2 layer 36, which acts as a partial barrier to penetration of the unfocused ion dosage.

A solid phase epitaxy process (SPE) at about 500-700°C in N_2 or Ar is then employed to transform the amorphous strips 42 to single crystal Si by regrowth from both sides of the amorphized region. (Step 9 Fig 6). The lateral growth rate for Si (undoped) is given by the following equation:

$$\mu \text{ (growth rate)} = 2.89 \times 10^8 \exp\left(\frac{-2.68 \pm 0.05 eV}{kT}\right) cm/sec$$

where k=Boltzmann's constant and T=absolute temperature in °K. Solving this equation at 550°C annealing temperature, μ = 1Å/sec. For a 3 micron

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strip, about 5 hours are required for lateral growth from both sides at 550°C. Using this process of entrainment, followed by implantation and SPE from defect-free areas, the sub-boundaries and crystal defects have been eliminated. (See Fig. 7). Figure 7 is a transmission electron micrograph of an area of Si film (labelled C) or SiO_2 (labelled A) wherein after ion-implantation and SPE, no defects were observed; whereas there were dislocations before said treatment in this area.

One can also use rapid thermal annealing to perform SPE. In this case, the growth rate at 1100°C can be over tens of microns per second.

Preferably, the structure is then processed by removing the remaining SiO_2 layer 36 (Step 10 Fig 6) and then edge cutting and thinning the wafer 10 (Step 11 Fig 6) to produce a defect-free SOI structure as shown in Fig 5.

Alternately, instead of entrapping defects with entrainment strips, it is possible to optically locate defects in ZMR films. The recrystallized Si films are found to have a slight thickness variation after zone melting. The Si thickness is usually different from the rest of the film in the regions of defect trails. Usually, the film is thinner, by about 100-200Å, in the regions of defect trails. This variation can be readily observed by optical microscope, especially in Nomalski or other interference contrast mode. With this observation,

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using optical microscopy, the defect trails can be located. Once located, a focussed ion implantation beam, such as an Si beam, can be directed to the defect region to amorphize these areas. Then the amorphized structure is regrown by SPE, as described above in connection with the strip embodiment. The SPE regrowth is seeded by the laterally adjacent single crystal regions on all sides of the amorphized region of the film, producing a substantially defect-free Si film.

In an alternative procedure, a semi-transparent mask can be placed over the zone-crystallized film. Because of the difference in thickness at the defect trails, an optical interference pattern is formed when the mask is illuminated by a collimated beam. This pattern is used to expose only the defect trail regions, which have different thicknesses than the rest of the film. One can then amorphize the defect trail regions, as previously described, and then SPE the defects, as also described above.

With either of the above two methods, or variations thereof, one can amorphize the defect trail regions automatically, without having to initially entrain them, and then locate the entrained regions.

The whole concept of ion-implanting defected areas of the film and then annealing the defects off is especially effective for thin films, such as below 2500Å. This is because it is much easier to amorphize a thin film by ion-implantation than a thicker film. For example, by using a 100 Kev Si

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beam, a 2500Å thick Si film can be amorphized.

In an experimental sample, ZMR silicon samples (Si layer 3000Å thick) were implanted with $^{30}Si+$ at an energy of 180 KeV to a dose of $7x10^{14}/cm^2$. This dose amorphized almost the entire layer within which defects, such as dislocations, lose their identity. Solid phase epitaxial (SPE) regrowth in silicon has a considerably lesser activation energy (about 2.7 eV) compared to random nucleation and growth processes (the rate of random recrystallization characterized by an activation energy of about 3.9 eV). Consequently, at a growth temperature of 600°C, regrowth of a 3000Å layer takes place exclusively by solid phase epitaxial regrowth. The microstructure studies obtained after annealing at 600°C for 30 minutes showed no crystalline defects in regions, whereas there were defects before amorphization.

Equivalents

This completes the description of the preferred embodiments of the invention. While the invention has been particularly shown and described with reference to such embodiments, it should be understood that those skilled in the art will be capable of devising various changes in form and detail without departing from the spirit and scope of the invention. For example, a Si semiconductor film and substrate has been used in reference to the preferred embodiments. Other semiconductor materials are

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contemplated within the scope of the invention, such as compound semiconductors of III-V materials; in particular, GaAs or alloys thereof. Furthermore, the SiO_2 insulator may be replaced by other materials, such as sapphire, to produce an SOS structure instead of an SOI structure.

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CLAIMS

1. A method of zone melting and recrystallization of semiconductor film formed on an insulator over a silicon substrate comprising the steps of:

a. forming a protective capping layer over the semiconductor film;

b. zone melting and recrystallizing said film to transform said film to a single crystal, or nearly single crystalline structure;

c. locating and amorphizing regions in said film where crystalline defects are located while leaving single crystal or nearly single crystal regions laterally adjacent thereto;

d. laterally regrowing said amorphized structure to transform the amorphized structure to single crystal or nearly single crystal material seeded by the single crystal or nearly single crystal regions laterally adjacent thereto.

2. The method of Claim 1 further comprising the steps of edge cutting the structure formed after step c), regrowing the capping layer and thinning the structure.

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3. The method of Claim 1 wherein the capping layer is SiO_2, Si_3N_4 or both and the semiconductor film is Si.

4. The method of Claim 1 wherein said structure is annealed between steps b) and c) at a temperature between 1100°c and 1400°c.

5. A method of zone melting and recrystallization of polysilicon film formed on an insulator over a silicon substrate comprising the steps of:

a. forming a protective capping layer over the polysilicon film with a capping material;

b. forming strips in, or on, said capping layer of material having a melting point above that of silicon and capable of being etched;

c. zone melting and recrystallizing said polysilicon film to transform said polysilicon film to single crystal, or nearly single crystalline silicon structure with crystal defects primarily located beneath the strips;

d. forming openings at said strips to expose the underlying transformed silicon structure;

e. amorphizing the exposed underlying silicon structure leaving single crystal or nearly single crystalline material laterally adjacent the amorphized silicon structure;

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f. laterally regrowing said amorphized structure seeded by the single crystal, or nearly single crystal material laterally adjacent thereto.

6. The method of Claim 1 wherein strips are formed in, or on, the capping layer to localize crystalline defects in the semiconductor film.

7. A method of preventing wafer deformation comprising zone melting and recrystallization of a semiconductor material with a plurality of heat sources wherein the thermal gradient across the recrystallizing material is reduced such that the crystalline material has substantially reduced slip during recrystallization.

8. The method of Claim 7 wherein at least three heat sources are employed during recrystallization.

9. A method of reducing edge effects along a periphery of a semiconductor wafer comprising the step of removing a portion of the wafer along the periphery.

10. The method of Claim 9 wherein said removing step is comprised of cutting said portion with a laser.

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11. The method of Claim 9 wherein said removing step is comprised of sand blasting said portion to remove it from the wafer.

12. The method of Claim 9 wherein said removing step is comprised of grinding along the periphery.

13. A method of reducing edge effects along a periphery of a semiconductor wafer comprising the step of removing a portion of a surface of the wafer about the periphery.

14. The method of Claim 13 wherein said removing step is comprised of the ultrasonic machining of a portion of the surface.

15. The method of Claim 13 wherein said removing step is comprised of grinding the portion of the surface to be removed.

16. The method of Claim 13 wherein said removing step is comprised of sand blasting the periphery of the surface.

17. The method of Claim 13 wherein said removing step is comprised of chemical etching the periphery of the surface.

18. The method of Claim 13 wherein said removing step is comprised of dry etching the periphery of the surface.

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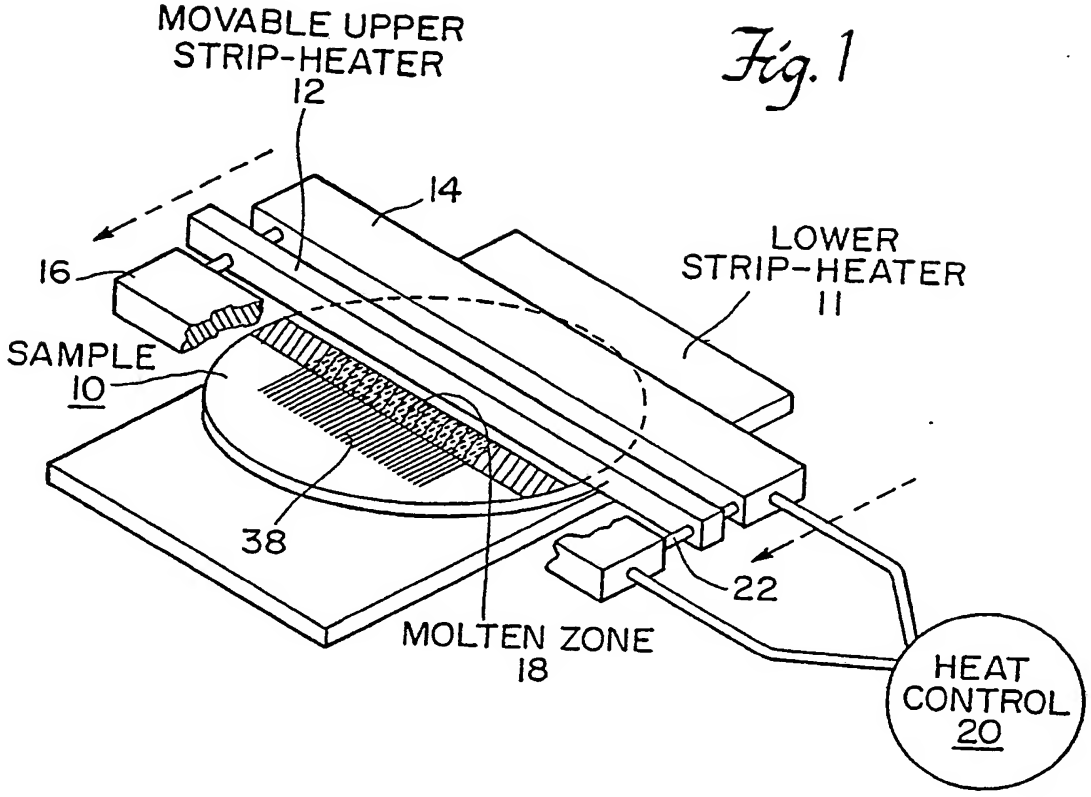

Fig. 1

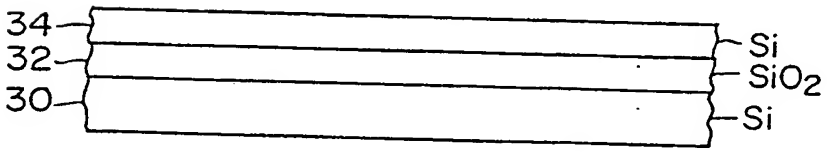

Fig. 2

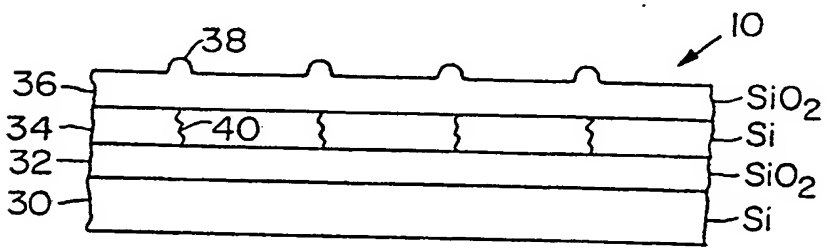

Fig. 3

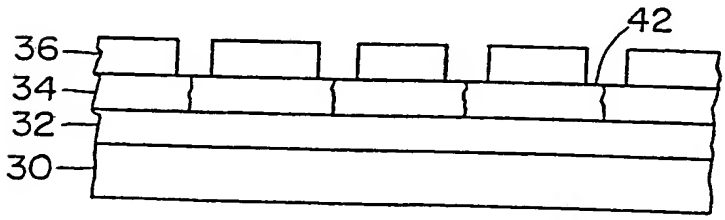

Fig. 4

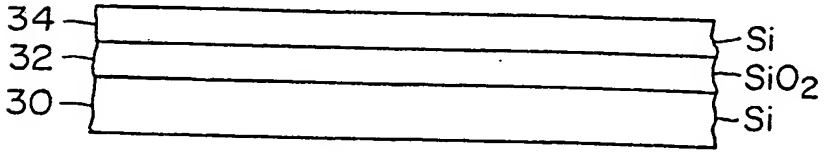

Fig. 5

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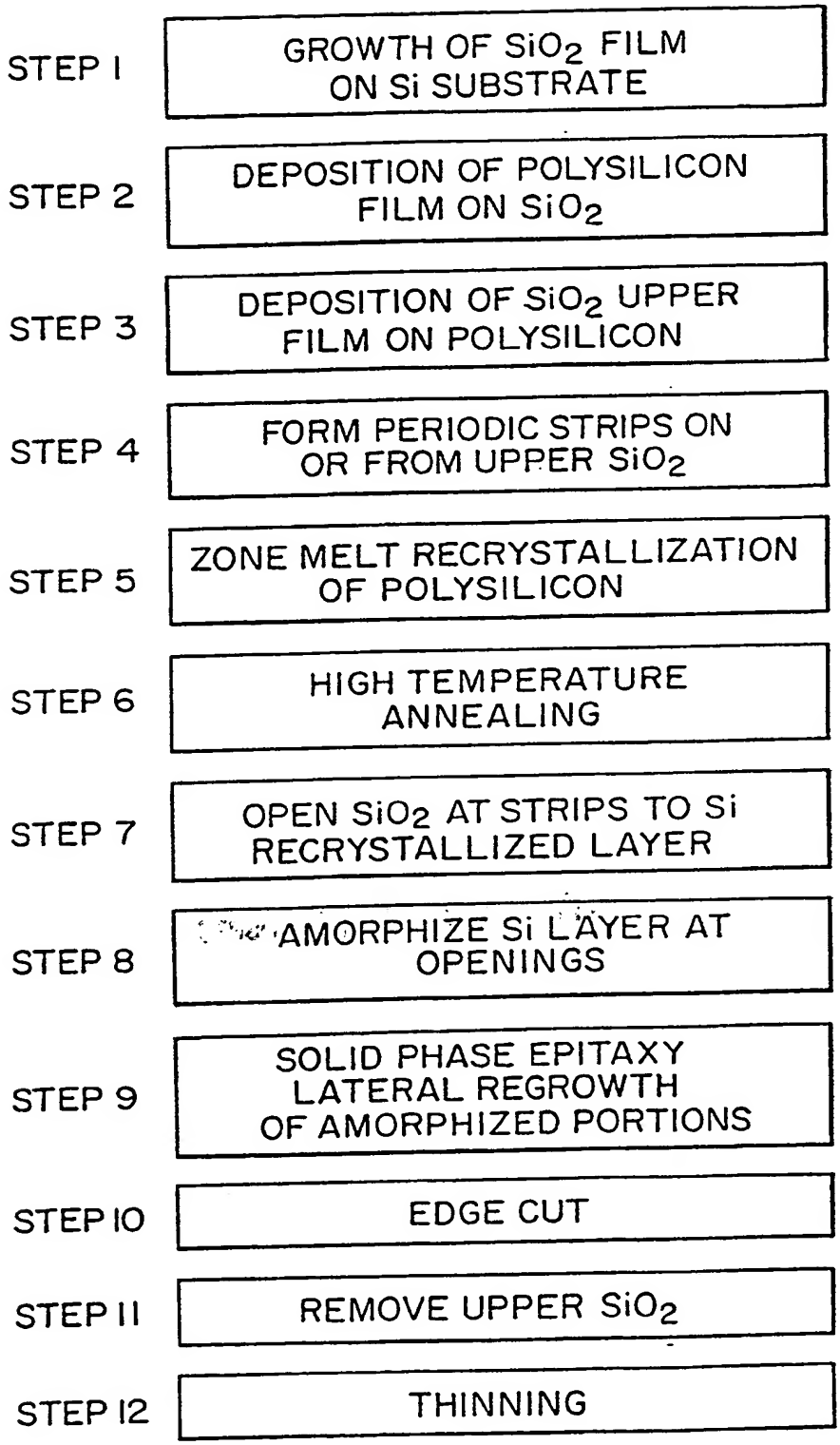

Fig. 6

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